METHOD AND APPARATUS FOR IMPLEMENTING AUTOMATED ELECTRONIC PACKAGE TRANSMISSION LINE CHARACTERISTIC IMPEDANCE VERIFICATION

Field of the Invention

The present invention relates to a method and apparatus for implementing automated electronic package transmission line characteristic impedance verification.

Description of the Related Art

For the design of transmission lines in electronic packages, one of the most critical parameters to control is the characteristic impedance Z_O. The characteristic impedance of transmission lines in electronic packages with high interconnect densities is most commonly measured using time-domain techniques such as time-domain reflectometry (TDR). TDR techniques assume a particular time-domain input excitation waveform, namely, a fast edge transition with a known rise time.

FIG. 1 illustrates the setup for such TDR characteristic impedance measurement techniques. The characteristic impedance is then calculated by analyzing the waveform at the near-end of the transmission line being tested.

The disadvantages of this approach include the following:

(A) Complex and expensive electronic test instrumentation is

required to generate and measure the input excitation waveform.

(B) Analysis of the transmission line's near-end waveform is relatively complex and requires subjective analytic interpretation, and thus is often not convenient for a production manufacturing environment.

(C) The time-domain input signal has multiple frequency components, leading to an inherent ambiguity in the frequency at which the characteristic impedance measurement was performed.

Other known techniques for measuring characteristic impedance of a transmission line use a frequency-domain approach, featuring an excitation waveform with only a single sinusoidal frequency component. Such techniques have the advantage of measuring the characteristic impedance at one particular frequency of interest.

FIGS. 2A and 2B illustrate the setup for one such frequency-domain technique that involves two measurements of the input impedance of a transmission line. The first measurement is done with the transmission line terminated in an open circuit as shown in FIG. 2A. The second measurement is done with the transmission line terminated in a short circuit as shown in FIG. 2B.

Typically, the technique illustrated in FIGS. 2A and 2B has been applied in a laboratory environment to discrete transmission line structures, such as coaxial cables, and not in a production test environment to electronic packages with high interconnect densities, i.e., those with multiple transmission line structures.

A need exists for an effective mechanism for implementing automated electronic package transmission line characteristic impedance verification.

Summary of the Invention

A principal object of the present invention is to provide a method and apparatus for implementing automated electronic package transmission line characteristic impedance verification. Other important objects of the present

invention are to provide such method and apparatus for implementing automated electronic package transmission line characteristic impedance verification substantially without negative effect and that overcome many of the disadvantages of prior art arrangements.

In brief, a method and apparatus are provided for implementing automated electronic package transmission line characteristic impedance verification. A sinusoidal voltage source is coupled to a transmission line test structure for generating a selected frequency. Impedance measuring circuitry is coupled to the transmission line test structure for measuring an input impedance with an open-circuit termination and a short-circuit termination. Characteristic impedance calculation circuitry is coupled to the impedance measuring circuitry receiving the input impedance measured values for the open-circuit termination and the short-circuit termination for calculating characteristic impedance. Logic circuitry is coupled to the characteristic impedance calculation circuitry for comparing the calculated characteristic impedance with threshold values for verifying acceptable electronic package transmission line characteristic impedance.

Brief Description of the Drawings

The present invention together with the above and other objects and advantages may best be understood from the following detailed description of the preferred embodiments of the invention illustrated in the drawings, wherein:

FIG. 1 is a schematic diagram illustrating a prior art time-domain reflectometry (TDR) characteristic impedance measurement technique;

FIGS. 2A and 2B are diagrams illustrating prior art frequency-domain characteristic impedance measurement technique;

FIGS. 3 and 4 are schematic diagrams illustrating alternative apparatus for implementing automated electronic package transmission line characteristic impedance verification in accordance with the preferred embodiments; and

FIG. 5 illustrates an electronic unit in accordance with a preferred embodiment of the apparatus of FIGS. 3 and 4.

Detailed Description of the Preferred Embodiments

In accordance with features of the preferred embodiment, a method is provided for verifying an electronic package's characteristic impedance through the utilization of a single electronic integrated circuit device, thereby making its measurement very repeatable and easily interpretable in a production manufacturing environment.

Having reference now to the drawings, two embodiments of the invention are provided and illustrated in FIGS. 3 and 4. In FIG. 3, there is shown apparatus for implementing automated electronic package transmission line characteristic impedance verification generally designated by the reference character 300 in accordance with one preferred embodiment. In FIG. 4, there is shown apparatus for implementing automated electronic package transmission line characteristic impedance verification generally designated by the reference character 400 in accordance with another preferred embodiment. In both embodiments 300, 400, one or more test traces are built into the electronic package design and then internal circuitry of an electronic integrated circuit respectively defining apparatus 300 or apparatus 400 analyzes these traces to actively determine the characteristic impedance.

Both apparatus 300 and apparatus 400 consolidate the various electronic components required for the method illustrated in FIGS. 2A and 2B into a single integrated circuit device. Both apparatus 300 and apparatus 400 allow electronic package transmission line characteristic impedance verification in an automated fashion and in a production or manufacturing environment.

Apparatus 300 has the advantage of a simpler integrated circuit (IC) design, at the expense of possible losses in accuracy due to variation between the two required transmission line test structures, implemented at the package level with open-circuit termination and short-circuit terminations, respectively. Apparatus 400 has the advantage of greater accuracy due to

the requirement of only a single transmission line test structure, at the possible expense of a more complicated IC design due to the addition of circuitry for providing the required open-circuit termination and short-circuit termination, in a sequential manner and the like.

Apparatus 300 of the preferred embodiment consolidates electronic components into an integrated circuit including an open circuit (Z_{oc}) impedance measuring circuitry 302, a short circuit (Z_{sc}) impedance measuring circuitry 304, and a respective associated sinusoidal voltage source 306, 308. Apparatus 300 includes a characteristic impedance calculation block 310 coupled to the impedance measuring circuitry 302, 304 receiving the input impedance measured values Z_{oc} and Z_{sc} for calculating characteristic impedance Z_o.

From transmission line theory, it is known that for a given line of length l.

$$Z_{oc} = Z_o \coth (\alpha + j\beta)*l, \text{ and}$$

$$Z_{sc} = Z_o \tanh (\alpha + j\beta)*l$$

Then the characteristic impedance Z_o, is calculated from the measured values of input impedance measured values Z_{oc} and Z_{sc}, as follows:

$$Z_o = (Z_{sc} \cdot Z_{oc})^{1/2}$$

One significant advantage of this method for calculating the characteristic impedance Z_o at characteristic impedance calculation block 310 of apparatus 300 is that it inherently accounts for transmission line attenuation and dispersion mechanisms, i.e., lossy lines are automatically covered.

Apparatus 300 includes logic circuitry 312 coupled to the characteristic impedance calculation block 310 receiving the calculated characteristic impedance Z_o and control tolerances Z_1, Z_2 representing the limits of the characteristic impedance specification are required inputs. A simple pass/fail criteria, represented by $Z_1 < Z_o < Z_2$, is implemented by

logic circuitry 312 and the pass/fail results are displayed by a display 314, which allows any operator on the production floor to easily verify the particular package meets the specification. For example, display 314 is implemented by pair of light emitting diodes (LEDs) to display the pass or fail result.

Referring to FIG. 4, apparatus 400 includes an impedance measuring circuitry 402 coupled to an open circuit and short circuit termination circuitry 404, and a sinusoidal voltage source 406. Apparatus 400 includes a characteristic impedance calculation block 408 coupled to the impedance measuring circuitry 402 receiving the input impedance measured values Z_{oc} and Z_{sc} for calculating characteristic impedance Z_o. Apparatus 400 includes logic circuitry 410 coupled to the characteristic impedance calculation block 408 receiving the calculated characteristic impedance Z_o and control tolerances Z_1, Z_2 representing the limits of the characteristic impedance specification are required inputs. A simple pass/fail criteria, represented by $Z_1 < Z_o < Z_2$, similarly is implemented by logic circuitry 410 and the pass/fail results are displayed by a display 412.

Referring to FIG. 5, there is shown an electronic unit generally designated by the reference character 500 in accordance with a preferred embodiment. Electronic unit includes a single integrated circuit device 502 and a card or multi-chip module 504. In apparatus 300, the single integrated circuit device 502 includes the impedance measuring circuitry 302, 304; the sinusoidal voltage sources 306, 308; the characteristic impedance calculation block 310, logic circuitry 312, and display 314. In apparatus 400, the single integrated circuit device 502 includes the impedance measuring circuitry 402; the open circuit and short circuit termination circuitry 404, sinusoidal voltage source 406,characteristic impedance calculation block 408, logic circuitry 410, and display 412. A transmission line test structure 506 representing conductors on the card or multi-chip module 504 respectively defines the transmission line test structures #1, #2 of FIG. 3 or the single transmission line test structure of FIG. 4. The single integrated circuit device 502 of apparatus 300 and of apparatus 400 is located on or is included in the card or multi-chip module 504 for the respective transmission line test structures.

Several advantages of the method of the invention implemented with apparatus 300 and apparatus 400 over the commonly used time-domain method of FIG. 1 include the following:

(A) Expensive test instrumentation is no longer needed on the production floor to verify that transmission lines meet the required characteristic impedance requirement.

(B) Any test inconsistencies between equipment and equipment operators are eliminated, as well as subjective analysis of the results.

(C) The characteristic impedance can be measured and validated at single, discrete frequency(ies) of interest, i.e., the ambiguities in frequency content inherent in time-domain methods are eliminated.

While the present invention has been described with reference to the details of the embodiments of the invention shown in the drawing, these details are not intended to limit the scope of the invention as claimed in the appended claims.